System Reduction for Nanoscale IC Design (SyreNe)

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1 Introduction

Since 1993, the German Federal Ministry of Education and Research (BMBF – *Bundesministerium füa Bildung und Forschung*) runs a program for supporting applied mathematical research. Projects funded through this BMBF program on the one hand aim at solving real-world application problems while on the other hand at advancing basic mathematical research. The fifth funding period (July 1, 2007 – June 30, 2010) of the BMBF applied mathematics program, titled *Mathematik für Innovationen in Industrie und Dienstleistungen (Mathematics for Innovations in Industry and Services)* was announced in May 2006. The call for proposals named a variety of research areas in applied mathematics as well as application fields. One of the listed mathematical research areas was *System Reduction and Algorithms for High-Dimensional Problems*, the application areas included the field of *Nanoelectronics*. An increasingly important and world-wide active research field at the intersection of these topics is model order reduction (MOR) for circuit simulation [7]. As the enhancements of methods and algorithms in this area is of major interest to several semiconductor industries operating in Germany, such as *Infineon Technologies* and *Qimonda* in Munich and the *NEC Laboratories Europe* in St. Augustin, several German research groups and the named companies joined forces in a proposal for the research network *System Reduction for Nanoscale IC Design (SyreNe)*. Besides the abovementioned companies, the SyreNe partners are

- TU Berlin/MATHEON, research group *Scientific Computing* (Dr. Tatjana Stykel),
- TU Braunschweig, Institut *Computational Mathematics* (Prof. Dr. Heike Faßbender and Prof. Dr. Matthias Bollhöfer),
- TU Chemnitz, research group *Mathematics in Industry and Technology (MiIT)* (Prof. Dr. Peter Benner, SyreNe coordinator),
- University of Hamburg, research group *Optimization of Complex Systems* (Prof. Dr. Michael Hinze),
- Fraunhofer Institut für Techno- und Wirtschaftsmathematik (ITWM) Kaiserslautern, Department *System Analysis, Prognosis and Control* (Dr. Patrick Lang).

In the following, we will give an overview of the goals of the research network and the six funded projects within SyreNe.

2 Goals of SyreNe

The ever decreasing feature size of integrated circuits (ICs) has lead to structures on the nanoscale. Current CPUs are produced using 45nm technology. We are on the verge of 32nm technology and 22nm technology is under development. Although we have not fully reached nanoelectronics which is often defined to start at 11nm[1], we are facing nanoscale structures. This development is accompanied by increasing numbers of devices and circuit elements as well as packaging density. As a consequence, the effects of interconnect and power grid on the physical behavior of ICs can no longer be neglected. Moreover, critical semiconductor devices may no longer be replaced by an equivalent circuit model, but need to be described by complex mathematical models like drift-diffusion (DD) [3]. Together with shorter design cycles, the increased modeling complexity leads to significant

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[1] See http://en.wikipedia.org/wiki/11nm.

challenges in the development of ICs. Circuit simulation is an indispensable tool in the design and verification of new layouts as prototyping is to be minimized due to the prohibitive photomasking costs. Thus, numerical algorithms need to be used to test and validate all essential circuit properties in computer simulations.

The physical behavior of ICs is usually described by a system of coupled differential-algebraic equations (DAEs) and partial differential equations (PDEs). The DAE part mainly consists of the circuit equations derived usually by modified nodal analysis (MNA), while the PDE parts arise, e.g., from the DD device models. The numerical treatment of this coupled system leads to hundreds of millions of equations and variables. Thus, a full numerical simulation of such problems with nowadays computing technology is by far too expensive with respect to computing times and memory requirements. Therefore, methods of system reduction (also: model order reduction, dimension reduction, see [1, 2, 6]) are of vital importance. These methods are used to reduce the complexity of the simulation by finding numerically approximations to the DAE and PDE systems that are much faster to simulate, require a lot less memory, but at the same time contain the essential information of the IC behavior. In order to reach these goals, the approximation errors need to be controlled and important system properties like stability and passivity need to be preserved in the reduced-order model.

The goal of SyreNe is to design methods for system reduction of high-dimensional models of nanoelectronic ICs. The methods are to be compared, benchmarked, tested and validated for practical examples provided by the semiconductor industry. For this purpose, we pursue two complementary approaches:

- Reduction of fully coupled systems using global methods ("couple-then-reduce");
- computation of reduced-order models of subcircuits and devices which are then coupled ("reduce-then-couple").

To this end, new methods for nonlinear MOR and for the reduction of systems with massive numbers of terminals like, e.g., power grids or clock-distribution networks [4, 5], are to be developed. Furthermore, computer algebra based methods are advanced by integrated PDE-based models and by developing suitable coupling mechanisms for numerical and symbolic system reduction techniques.

Together with the development and analysis of model reduction methods for circuit (P)DAE systems, the implementation of the algorithms, their integration into simulation packages of industrial partners and testing on practical problems are also part of the work program.

3 The Research Projects

The sub-projects SP1–SP6 within SyreNe focus on individual aspects of the research goals. These will be described in the following subsections. The projects interact with each other and with the industrial partners. A schematic overview of the interaction and dependencies within SyreNe is shown in Figure 1.

SP1: Model Order Reduction for Coupled Systems of ICs *(U Hamburg/M. Hinze)*

In this project, it is intended to reduce coupled nonlinear models consisting of (sub)circuit and devices (after suitable discretization) at once. From a practical point of view, the reduction of the system as a whole is of interest, because the allocation of the level of approximation between the different components of the circuit is left to the reduction method.

A circuit containing semiconductor components serves as raw model in this project. The semiconductor components in a first step are described by an instationary DD model. The coupling of the DD models with the circuit results in a PDAE system. Semi-discretization in space leads to a high-dimensional structured DAE system, whose numerical solution involves very high computational costs. The instationary PDAE system is reduced by a snapshot-POD.

The approach will be compared with the "reduce-then-couple" approaches in SP2–SP4 and interacts with SP5 on the aspects of coupling mechanisms between circuit descriptions and PDE models.

SP2: Passivity Preserving Model Reduction for Nonlinear DAEs
(TU Braunschweig/H. Faßbender)

In the MOR process it is crucial to preserve the acting properties of the initial system. This is particularly important if subsystems of complex

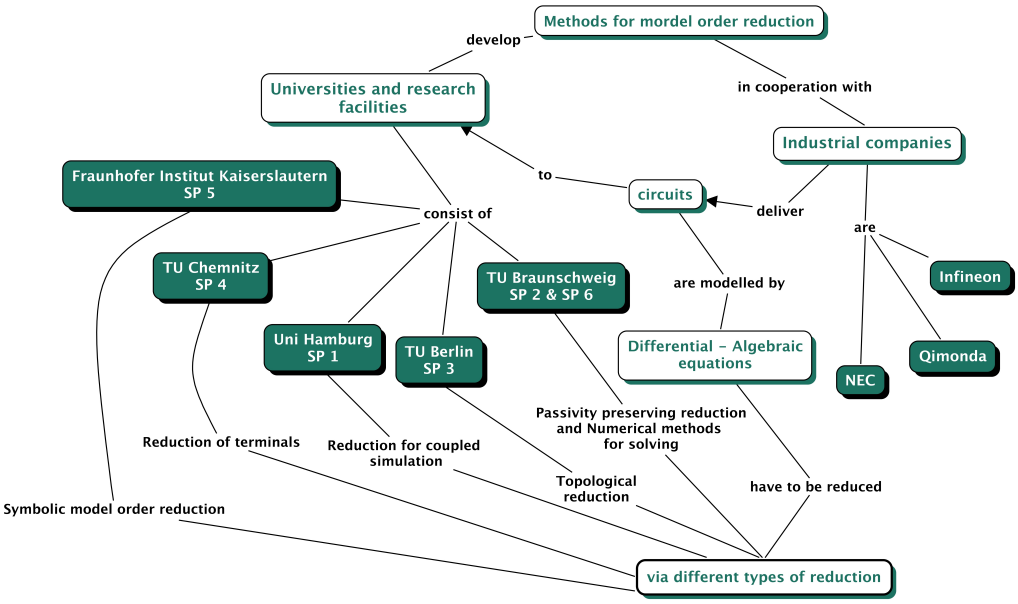

Figure 1: Interaction chart of SyreNe projects and industrial partners.

microsystems are considered whose acting properties determine the behavior of the complete system. One of these properties of non-driven subsystems is the so-called passivity. The goal of this project is the development of a passivity-preserving MOR method for non-linear DAEs stemming from MNA. The resulting reduced-order system should have a meaningful physical interpretation to allow for the use of usual CAE tools. In addition, a direct numerical simulation of the input-output behavior at significantly lower cost should be possible. SP2 interacts with SP3 on the exploitation of typical structures arising in DAE systems obtained by MNA.

SP3: Element-Based Model Reduction in Circuit Simulation *(TU Berlin/T. Stykel)*

The main objective of this project is to exploit the special topological structure and physical properties of electrical circuits to develop efficient system reduction methods for circuit equations. Passivity-preserving model reduction methods for linear (sub)circuit equations based on positive real and bounded real balancing will be developed. These methods require the availability of certain spectral projectors associated to the DAE system. The circuit topology will be used to compute these projectors efficiently. Furthermore, the influence of reduction of linear subsystems and power grids (see SP4) on the behavior of the nonlinear overall system will be investigated. Another step will be the investigation to what extent the topological structure of electrical circuits can be used in order to reduce the computational cost of the system reduction methods developed in SP2 for nonlinear DAEs.

SP4: Reduced Representation of Power Grid Models *(TU Chemnitz/P. Benner)*

Due to the constant decrease of IC feature sizes it becomes increasingly important to include the power supply of the electronic devices in the mathematical models used for simulation in the design and verification phase. The so-called "power grid" forms own layers within multilayer ICs. In power grid modeling, the system description leads to a huge number of inputs and outputs (terminals), since for every power-supplied element one pin as input and output appears. Most of the MOR approaches are based on the assumption that there are just a few inputs and outputs. Hence, new approaches are needed that can deal with the massive numbers of terminals.

The approach pursued in this project is based on compressing the input-/output matrices in such a way that the I/O behavior can be realized through as few virtual inputs/outputs as possible. Several numerical algorithms for computing these virtual terminals are investigated.

With the virtual input-/output matrices, standard MOR techniques like balanced truncation can be used for the resulting system. As besides the usual MOR approximation error, a second source of error results from the terminal compression, new error bounds need to be derived for controlling the quality of the reduced-order models.

SP5: Coupling of numeric/symbolic reduction techniques for the generation of parameterized models of nanoelectronic systems *(ITWM Kaiserslautern/P. Lang)*

In general, complex technical systems like the here considered nanoelectronic systems consist of different components, which are coupled according to a certain topology. Depending on the accuracy demands, there exist a variety of different models for the semi-conductor elements, which may be modeled as DAE or PDE descriptions in different complexity levels. The complete system — resulting from the coupling of the subsystems — thus has an hierarchical structure. This project has the goal to exploit this hierarchical structure and to perform the reduction of the overall system by systematically applying certain numerical or symbolic reduction techniques to appropriate subsystems. For this, the exploitation of the hierarchical structure is mandatory. Thus, the symbolic modeling process will be extended for the handling of hierarchical systems. This will then offer an opportunity for a decomposition of the system equations into several smaller subproblems and a coupling part. Thus, this procedure allows for an application of different solving and approximation methods to the corresponding subproblems, in particular those developed in SP2–SP4 can be employed. In this manner, the reduced-order systems finally can be rearranged to a reduced behavioral model and translated into an adequate behavioral description language (e.g. VHDL-AMS, Verilog-A).

Moreover, it will be investigated if the nonlinear symbolic approximation techniques that have been developed for DAE systems up to now, are applicable to discretized descriptions of PDE models like those used in SP1. Mechanisms for the DAE-PDE-coupling are developed jointly with SP1.

SP6: Numerical Solution of Systems of Equations and Coupling of Components in Model Order Reduction
(TU Braunschweig/M. Bollhöfer)

In this project, the focus is on solving unstructured systems arising from MOR. This is a common challenge for all projects within SyreNe. Furthermore, interfaces between the single application problems, as well as interfaces for simulation tools, will be provided. Due to the circuit topology, systems arising from circuit simulation consist of structures that require an adapted treatment. Therefore, methods like multigrid method as they are used for PDEs are not applicable. Furthermore, these high dimensional systems impose limits on the computational time as well as on memory usage. The linear systems induced by Lyapunov equations as they arise in the balanced truncation MOR methods used in SP3, SP4 are characterized by tensor structures which are not preserved by direct solvers and this makes their solution even harder. One objective of this project is to combine direct solves for ADI-type iterations employed in solving Lyapunov equations with low-rank updates. Whenever a direct solution of the underlying linear systems is no longer possible, iterative methods have to be applied. Preconditioning methods based on algebraic multilevel-ILU techniques will be adapted for systems of equations arising within SyreNe.

4 Activities

A number of SyreNe members participated in the conference **Scientific Computing in Electrical Engineering (SCEE 2008)**, held September 28 – October 3 at Helsinki University of Technology, Finland. Apart from several contributed papers, the opening lecture *Advances in balancing-related model reduction for circuit simulation*[2] of this conference was given by the SyreNe coordinator Peter Benner.

Jointly with the EU Marie Curie Transfer-of-Knowledge project **O-Moore-Nice**[3], the workshop **Model Reduction for Circuit Simulation** was organized at the University of

[2] Available at `http://www.tu-chemnitz.de/mathematik/syrene/aktuell/talks.php`.

[3] See `http://www.tu-chemnitz.de/mathematik/industrie_technik/projekte/omoorenice.php` for details.

Hamburg, October 30–31, 2008. For the program and participants, visit `http://www.math.uni-hamburg.de/spag/zms/syrene/`. A post-conference book based on the invited and contributed lectures given at the workshop will be published by Springer-Verlag, series LECTURE NOTES IN ELECTRICAL ENGINEERING. A second workshop is planned for 2010.

For all further information please visit

`http://www.syrene.org`,

where more detailed descriptions of the individual projects together with contact information, publications, talks, etc. can be found.

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