Chapter 1

Introduction: Part I

Why Parallel Computing?

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1. **Problem size exceeds desktop capabilities.**
2. **Problem is inherently parallel (e.g. Monte-Carlo simulations).**
3. **Modern architectures require parallel programming skills to be optimally exploited.**

Flynn's Taxonomy of Parallel Architectures

[Flynn '72]

The basic definition of a parallel computer is very vague in order to cover a large class of systems. Important details that are not considered by the definition are:

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- How many processing elements?
- How complex are they?
- How are they connected?
- How is their cooperation coordinated?
- What kind of problems can be solved?

The basic classification allowing answers to most of these questions is known as Flynn's taxonomy. It distinguishes four categories of parallel computers.

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3. Single-Instruction, Multiple-Data (SIMD)

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4. Multiple-Instruction, Multiple-Data (MIMD)

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Single-Instruction, Single-Data (SISD)

The SISD model is characterized by

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- **on a single piece of data,**
- **in each step of the execution.**

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Examples

- desktop computers until Intel® Pentium® 4 era,
- early netBooks on Intel® Atom™ basis,
- pocket calculators,
- abacus,
- embedded circuits

Flynn's Taxonomy of Parallel Architectures

Single-Instruction, Single-Data (SISD)

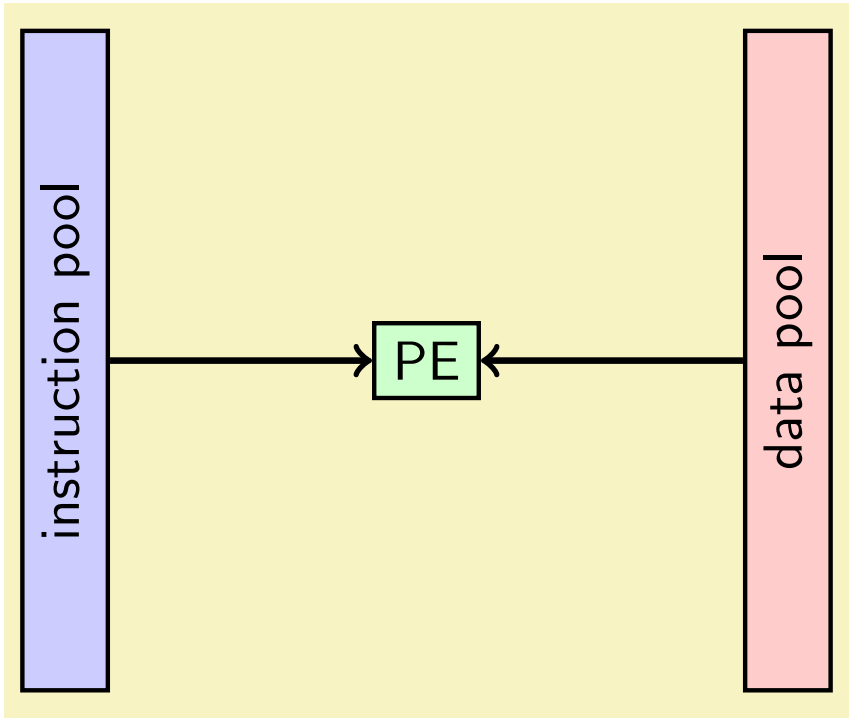

Figure: Single-Instruction, Single-Data (SISD) machine model

Flynn's Taxonomy of Parallel Architectures

Multiple-Instruction, Single-Data (MISD)

In contrast to the SISD model in the MISD architecture we have

- **multiple processing elements,**

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The MISD model is usually not considered very useful in practice.

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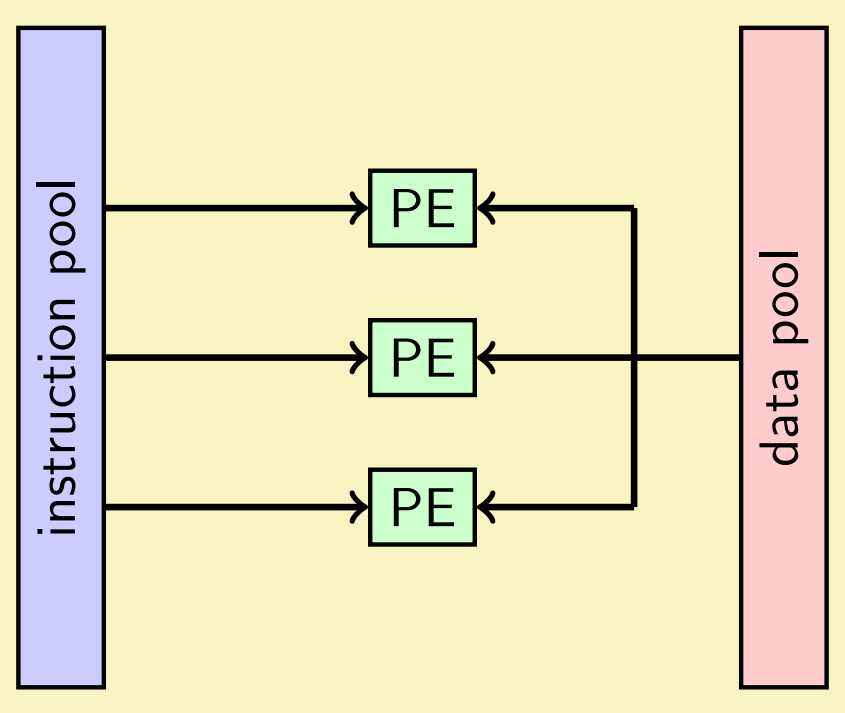

Figure: Multiple-Instruction, Single-Data (MISD) machine model

Flynn's Taxonomy of Parallel Architectures

Single-Instruction, Multiple-Data (SIMD)

Here the characterization is

- **multiple processing elements,**
- **execute the same instruction,**
- **on a multiple pieces of data,**
- **in each step of the execution.**

This model is thus the ideal model for all kinds of vector operations

$$c = a + \alpha b.$$

Examples

- Graphics Processing Units,
- Vector Computers,
- SSE (Streaming SIMD Extension) registers of modern CPUs.

Flynn's Taxonomy of Parallel Architectures

Single-Instruction, Multiple-Data (SIMD)

The attractiveness of the SIMD model for vector operations, i.e., linear algebra operations, comes at a cost.

Consider the simple conditional expression

```
if (b==0) c=a; else c=a/b;
```

The SIMD model requires the execution of both cases sequentially. First all processes for which the condition is true execute their assignment, then the other do the second assignment. Therefore, conditionals need to be avoided on SIMD architectures to guarantee maximum performance.

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Single-Instruction, Multiple-Data (SIMD)

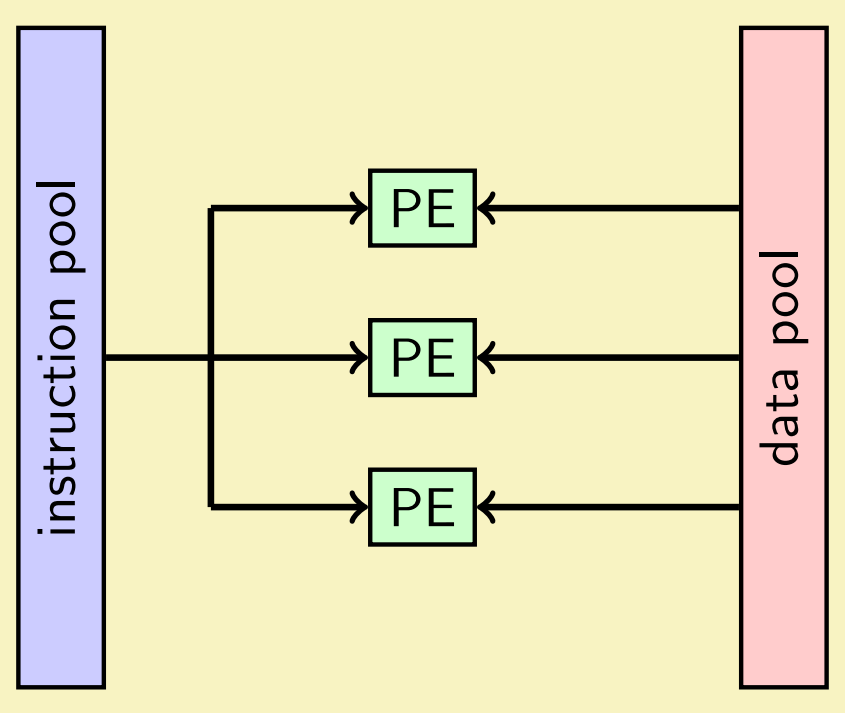

Figure: Single-Instruction, Multiple-Data (SIMD) machine model

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Multiple-Instruction, Multiple-Data (MIMD)

MIMD allows

- **multiple processing elements,**
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- **at each instance of time.**

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Examples

- multicore and multi-processor desktop PCs,
- cluster systems.

Flynn's Taxonomy of Parallel Architectures

Multiple-Instruction, Multiple-Data (MIMD): Hardware classes

MIMD computer systems can be further divided into three class regarding their memory configuration:

distributed memory

Every processing element has a certain exclusive portion of the entire memory available in the system. Data needs to be exchanged via an interconnection network.

shared memory

All processing units in the system can access all data in the main memory.

hybrid

Certain groups of processing elements share a part of the entire data and instruction storage.

Flynn's Taxonomy of Parallel Architectures

Multiple-Instruction, Multiple-Data (MIMD): Programming models

Single Program, Multiple Data (SPMD)

SPMD is a programming model for MIMD systems. "In SPMD multiple autonomous processors simultaneously execute the same program at independent points."[a] This contrasts to the SIMD model where the execution points are not independent.

[a] Wikipedia: `http://en.wikipedia.org/wiki/SPMD`

This is opposed to

Multiple Program, Multiple Data (MPMD)

A different programming model for MIMD systems, where multiple autonomous processing units execute different programs at the same time. Typically Master/Worker like management methods of parallel programs are associated with this class.

Flynn's Taxonomy of Parallel Architectures

Multiple-Instruction, Multiple-Data (MIMD)

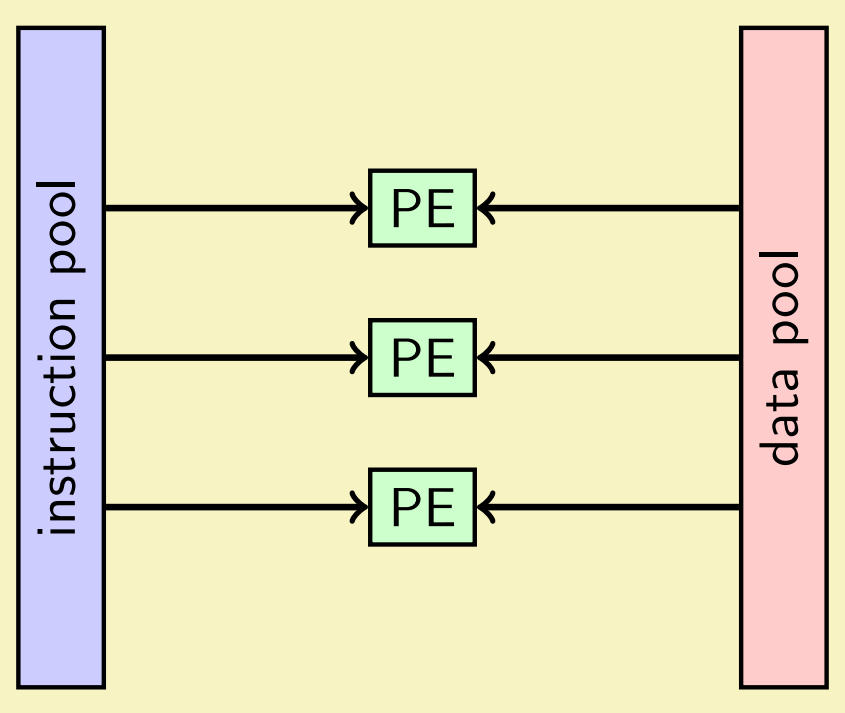


Figure: Multiple-Instruction, Multiple-Data (MIMD) machine model

Memory Hierarchies in Parallel Computers

Repetition Sequential Processor

- Cloud
- Network Storage
- Local Storage
  - Tape
  - Hard Disk Drive (HDD)
  - Solid State Disk (SSD)

slow and very slow

- Main Random Access Memory (RAM)

medium

- L3 Cache
- L2 Cache
- L1 Cache
- Registers

fast

Figure: Basic memory hierarchy on a single processor system.

Memory Hierarchies in Parallel Computers

Shared Memory: UMA

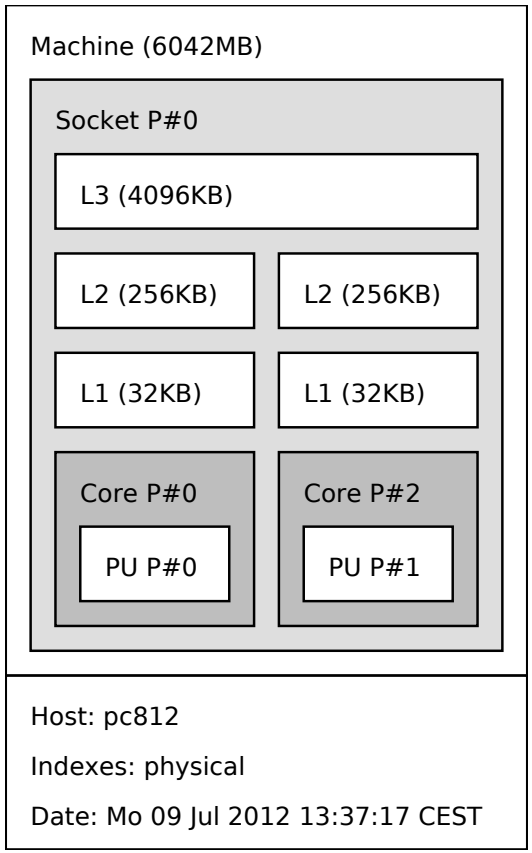


Figure: A sample dual core Xeon® setup

Memory Hierarchies in Parallel Computers

Shared Memory: UMA + GPU

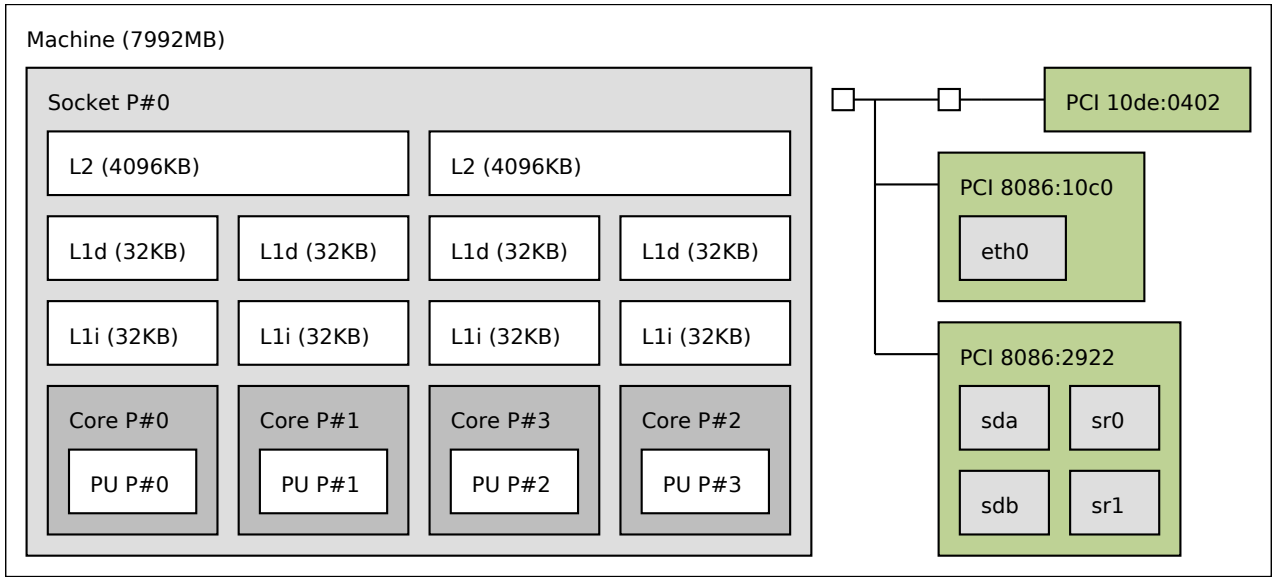


Figure: A sample Core™2 Quad setup

Memory Hierarchies in Parallel Computers

Shared Memory: NUMA

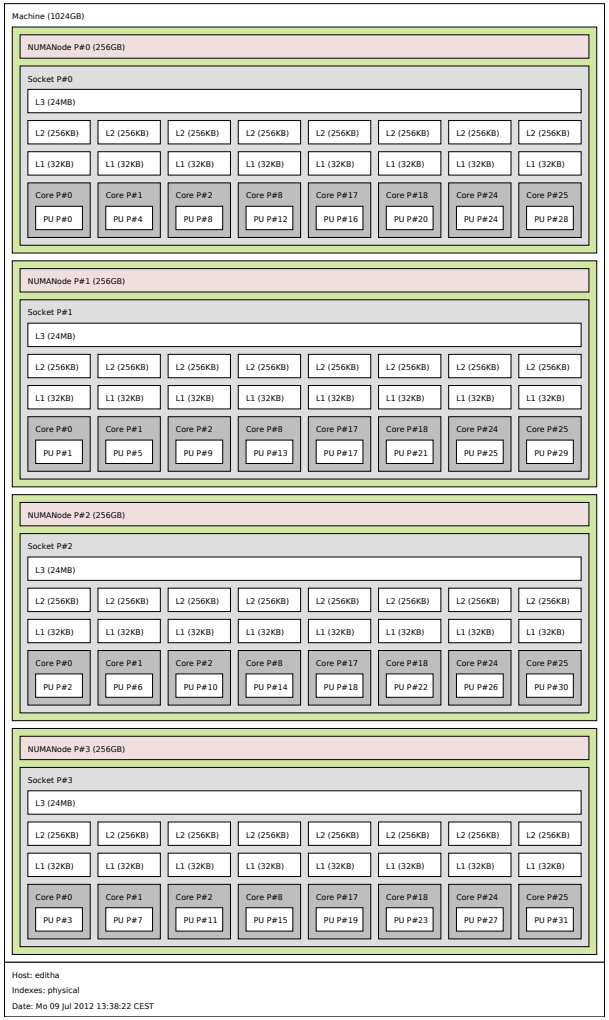
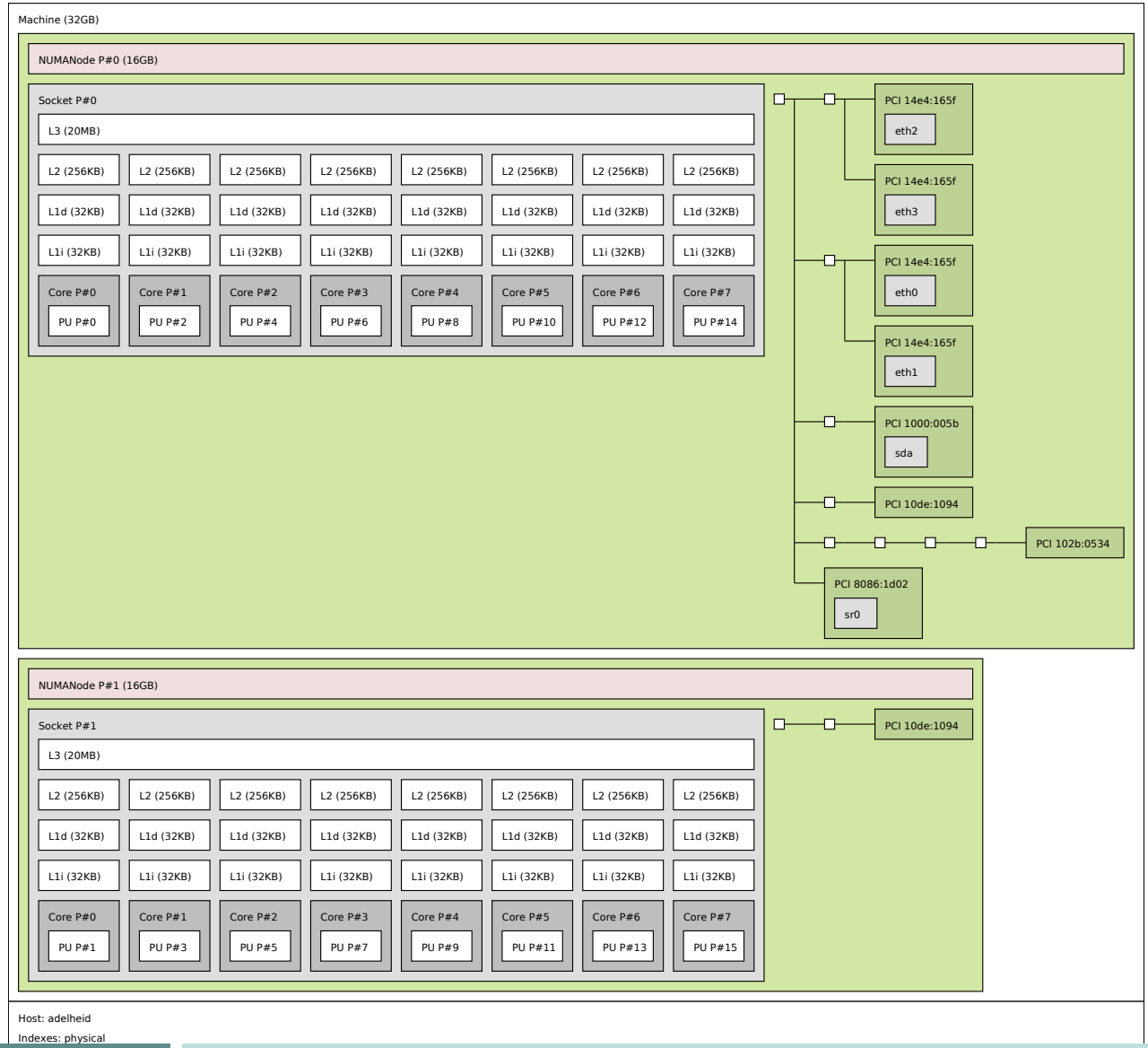


Figure: A four processor octa-core Xeon® system

Memory Hierarchies in Parallel Computers

Shared Memory: NUMA + 2 GPUs



Memory Hierarchies in Parallel Computers

General Memory Setting

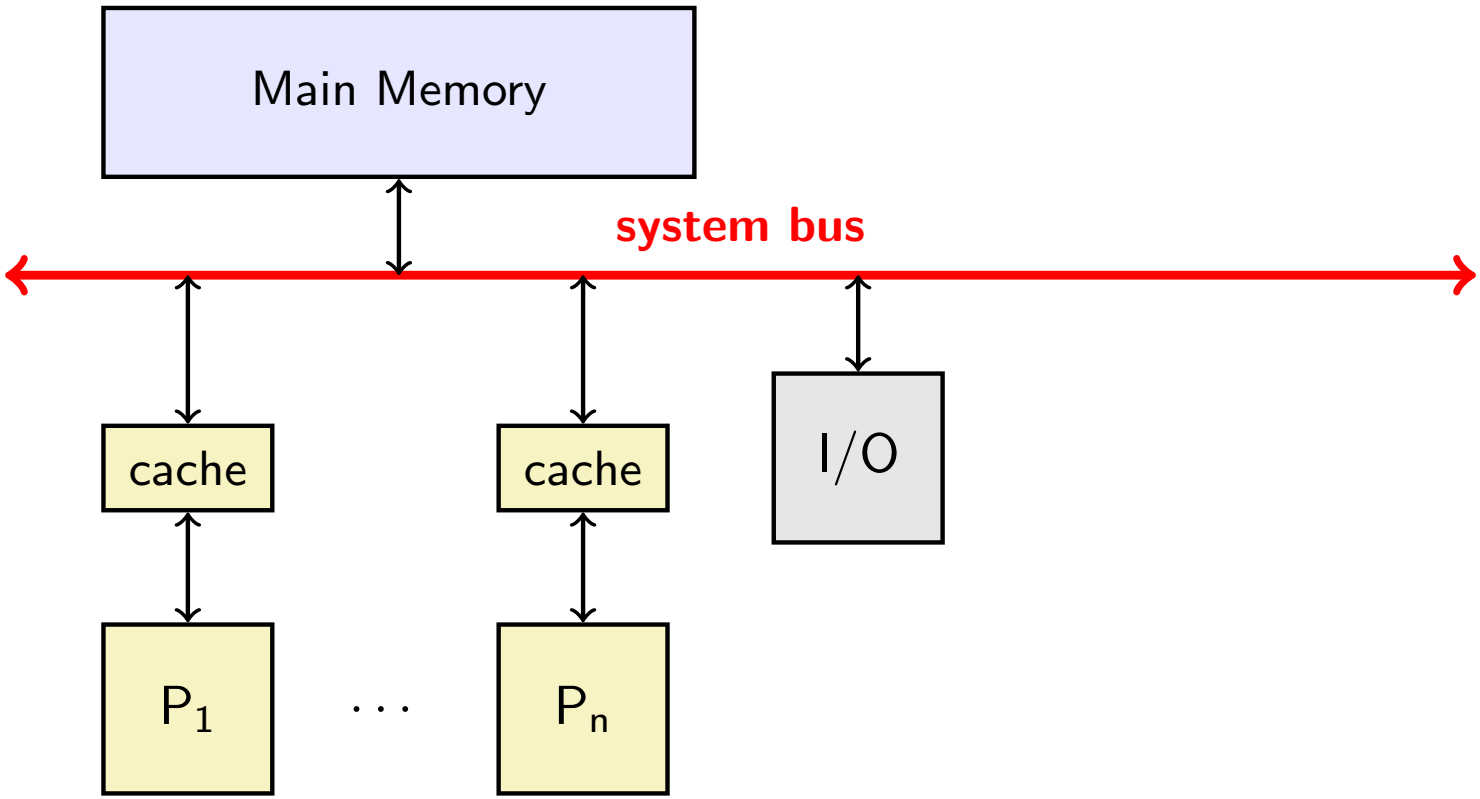


Figure: Schematic of a general parallel system

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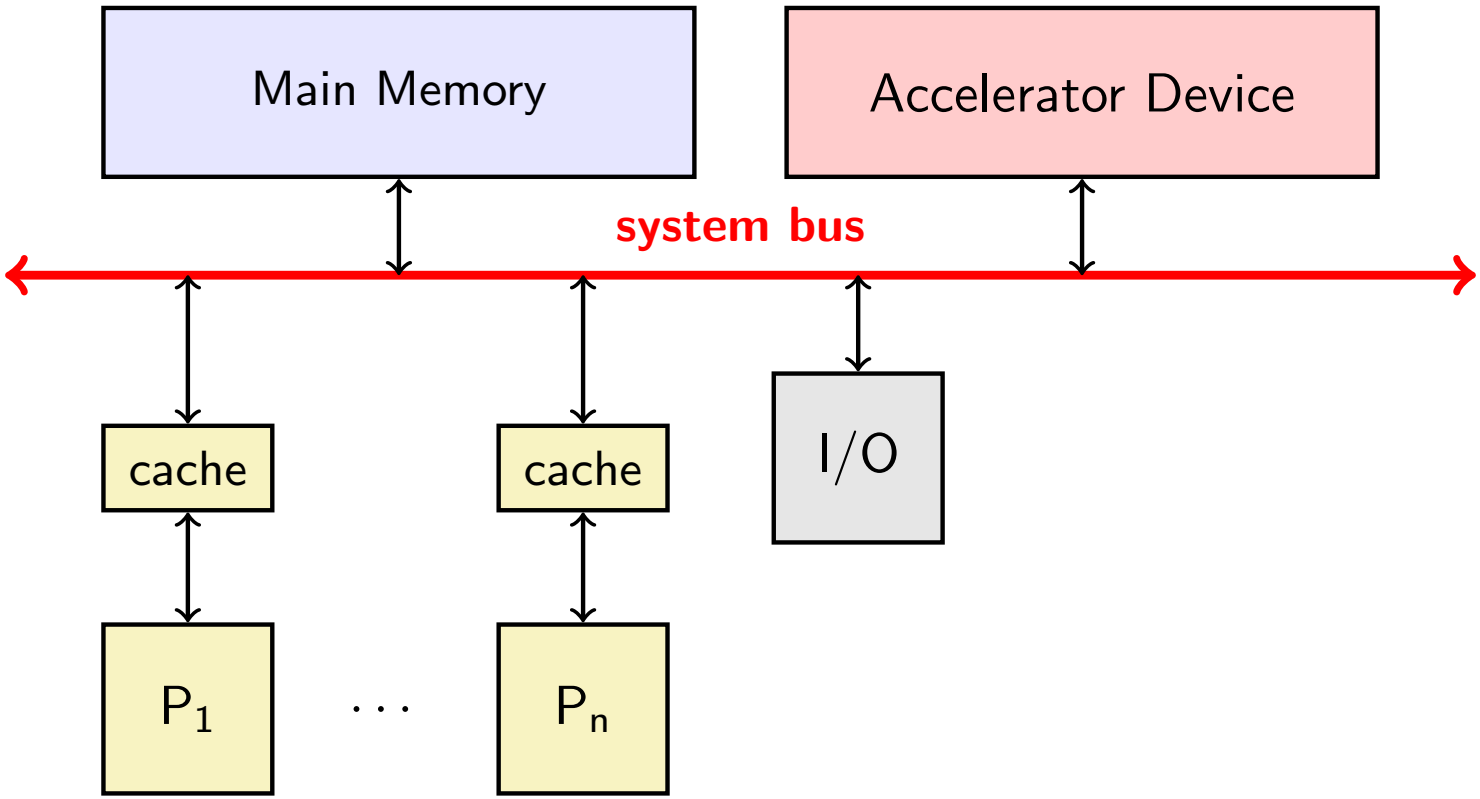

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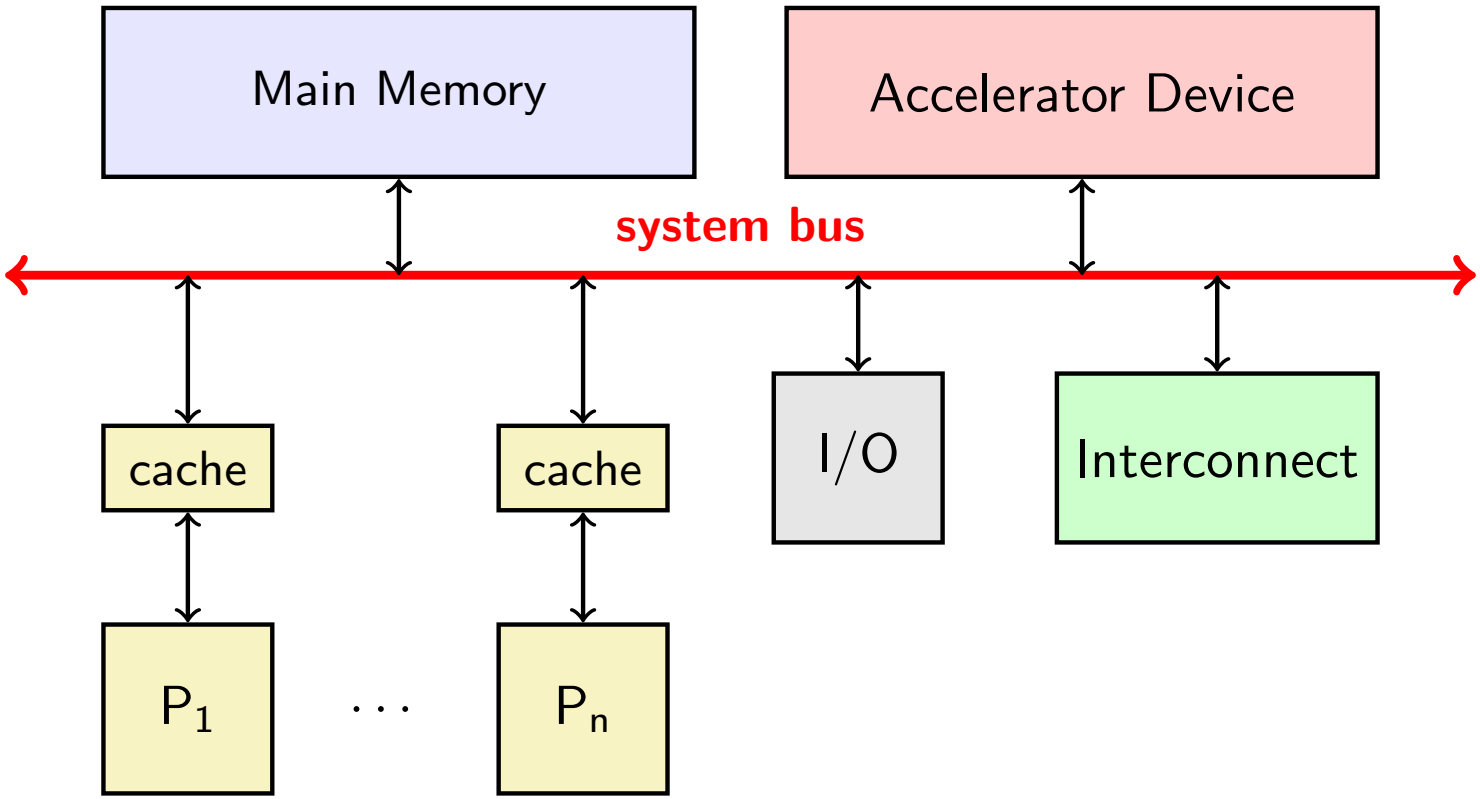

Figure: Schematic of a general parallel system

Communication Networks

The **Interconnect** in the last figure stands for any kind of Communication grid. This can be implemented either as

- **local hardware interconnect,**

or in the form of

- **network interconnect.**

In classical supercomputers the first was mainly used, whereas in today's cluster based systems often the network solution is used in the one form or the other.

Communication Networks

Hardware

MyriNet

- shipping since 2005
- transfer rates up to 10Gbit/s
- lost significance (2005 28.2% TOP500 down to 0.8% in 2011)

Infiniband

- transfer rates up to 300Gbit/s
- most relevant implementation driven by OpenFabrics Alliance[a], $\rightsquigarrow$ usable on Linux, BSD , Windows systems.
- features remote direct memory access (RDMA) $\rightsquigarrow$ reduced CPU overhead
- can also be used for TCP/IP communication

[a] http://www.openfabrics.org/

Communication Networks

Topologies

1. **Linear array:**
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4. **Mesh and Torus:**
   Every node is connected to a number of neighbours (2-4 in 2d mesh, 4 in 2d torus).

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5. **k-dimensional cube / hypercube:**
   Recursive construction of a well connected network of 2^k nodes each connected to k neighbors. Line for two, square for four, cube fore eight.

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6. **Tree:**
   Nodes are arranged in groups, groups of groups and so forth until only one large group is left, which represents the root of the tree.